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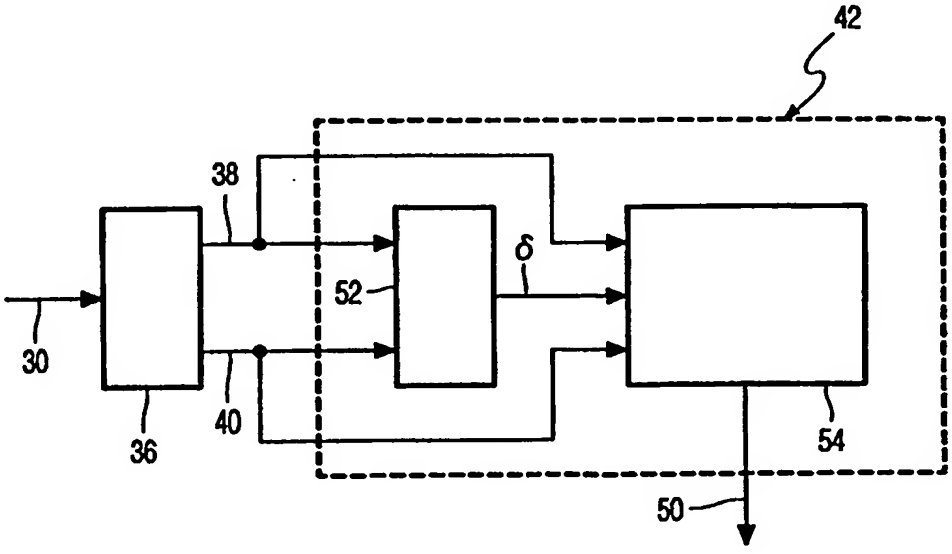
(54) Title: CLOCK RECOVERY CIRCUIT AND A RECEIVER HAVING A CLOCK RECOVERY CIRCUIT




(57) Abstract

A data receiver comprises receiving means for receiving a data signal and providing a base band output, demodulating means coupled to an output of the receiving means for providing a data output, and symbol recovery means (36, 42) coupled to an output of the demodulating means for recovering symbols represented by the data output. The symbol recovery means comprises means (52) for determining a time difference between rising and falling edges in the data output and their nominal reference points and means (54) for determining respective clock reference points for the rising and falling edges from the time difference between the rising and falling edges.

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DESCRIPTION

# CLOCK RECOVERY CIRCUIT AND A RECEIVER HAVING A CLOCK RECOVERY CIRCUIT

## Technical Field

The present invention relates to a clock recovery circuit, a receiver having the clock recovery circuit and a method of recovering a clock signal.

For convenience of description the present invention will be described with reference to a receiver.

## Background Art

In receivers used for receiving digital signals, such as pagers and cellular and cordless telephones, received signals are demodulated, decoded and transformed into Non-Return to Zero (NRZ) data of 1 or 2 bits. In order to make the information complete and suitable to be processed, a locally generated synchronisation clock is required. A clock recovery circuit is provided for generating this synchronisation clock.

US Patent Specification 5,418,822 discloses a circuit arrangement for generating a clock signal from a digital signal by evaluating signal edges of the digital signal. A first device generates a pulse at a signal edge oriented in a first direction, and a second device generates a pulse at a signal edge oriented in a second direction which is opposite to the first direction. Each of the devices has one terminal for receiving a digital signal and one output. A voltage-controlled, triggerable oscillator device has at least two trigger inputs, one control input and one output. Each of the trigger inputs is connected to the output of a respective one of the first and second devices, and the output of the oscillator device is an output for the clock signal. An integration device has an input connected to the output of the oscillator device and has an output connected to the control input of the oscillator device. The purpose of this circuit arrangement is to produce a clock signal that is synchronous in both frequency and phase with the clock signal that is fundamental to the data in the digital signal.

A disadvantage of clock recovery circuits which synchronise to the rise and fall edges is that if there are changes in the group delay of the transmitter then a relative shifting occurs between the rise and fall edges of the recovered data leading to jitter and loss of sensitivity in the generated clock signal.

Disclosure of Invention

An object of the present invention is to avoid loss of sensitivity in the clock recovery of a FSK signal.

According to one aspect of the present invention there is provided a receiver comprising receiving means for receiving a data signal and providing a base band output, demodulating means coupled to an output of the receiving means for providing a data output, and symbol recovery means coupled to an output of the demodulating means for recovering symbols represented by the data output, characterised in that the symbol recovery means comprises means for determining the occurrence of rising and falling edges in the data output, means for determining the differences between the occurrence of the rising and falling edges and means for utilising the differences for determining a clock reference position.

According to a second aspect of the present invention there is provided a clock recovery circuit comprising means for determining the occurrence of rising and falling edges in a data signal, means for determining the differences between the occurrence of the rising and falling edges and means for utilising the differences for determining a clock reference position.

In one embodiment of the present invention the means for determining a time difference between rising and falling edges in the data output and their nominal reference points produces a time difference signal. Additionally phase locked loop means (PLL) is provided having input means for the rising and falling edges and the time difference signal and means for calculating respective reference positions for the rise and fall edges.

By the phase locked loop means calculating the respective reference positions for the rising and falling edges, the phase locked loop means will not advance or retard for each symbol change because the rising and falling edges

are close to their respective calculated reference positions. As a result jitter due to different bit length is greatly reduced without decreasing the bandwidth of the phase locked loop means. The problem of the sensitivity degradation due to a difference in the bit length is solved without changing the bandwidth of the phase locked loop means. Additionally the frequency stability requirements on the phase locked loop reference oscillator are not stringent which permits the usage of less highly specified, cheaper crystals.

In a second embodiment of the present invention respective rising and falling edge phase locked loop means are provided for noting the occurrence of a respective edge position relative to a predetermined phase and averaging means are provided for determining a clock reference position from a circular mean of the phases in the respective phase locked loop.

According to a third aspect of the present invention there is provided a method of recovering symbols in a data signal, comprising determining the occurrence of rising and falling edges in the data signal, determining the differences between the occurrence of the rising and falling edges, and utilising the differences for determining a clock reference position.

Brief Description of Drawings

The present invention will now be explained and described, by way of example, with reference to the accompanying drawings, wherein:

Figure 1 is a simplified block schematic diagram of a selective call system,

Figure 2 is a simplified block schematic diagram of a clock recovery circuit,

Figure 3 is a vector diagram relating to a known type of phase locked loop (PLL),

Figures 4A and 4B show timing diagrams of originally generated symbols and of the same symbols as received by a secondary station, respectively,

Figure 5 is a simplified block schematic diagram of a clock recovery circuit for use in a receiver made in accordance with the present invention,

Figure 6 is a vector diagram of a substantially jitter free PLL,

Figure 7 is a block schematic diagram of another embodiment of the present invention,

Figure 8 illustrates a short symbol having errors δ/2 on its rising and falling edges, and

Figure 9 illustrates one method of averaging the current phases of the PLLs in Figure 7 and generating the recovered clock.

In the drawings the same reference numbers have been used to indicate corresponding features.

Modes for Carrying Out the Invention

The selective call system shown in Figure 1 comprises a primary station 10 having an input 12 for paging messages to be relayed to preselected users having secondary stations 20. The paging messages are encoded and formatted in a stage 14 and passed to a radio transmitter 16 for onward transmission as point-to-point paging signals. The operation of the primary station is controlled by a system controller 18.

The secondary station 20 comprises a receiver 22, for example a superheterodyne receiver or zero IF receiver, which frequency down converts the received signal to produce an output 24 comprising a bit sequence formed by single or pairs of bits or quadrature related I and Q signals at zero IF. The output 24 is applied to a base band stage 26 comprising a demodulator 28 which filters, decodes and transforms the output 24 into non-return to zero (NRZ) data 30 of 1 or 2 bits. A clock recovery circuit 32 generates a symbol clock signal from the NRZ data 30 and supplies the data and the symbol clock to a processor 34 in which the symbol value is derived by sampling the NRZ data 30 in the midway between the rising edge and falling edge.

Generally clock recovery relies on edge detection for synchronisation of a local clock signal with the received data, the edges corresponding to the changing of a data state. In selective call systems, such as a paging system operating in accordance with the CCIR Radiopaging Code No. 1, otherwise known as POCSAG, data corresponds to the frequencies of a frequency shift keyed (FSK) modulated radio signal.

A typical clock recovery circuit 32 is shown in Figure 2. The NRZ data 30 is applied to an edge detector 36 which provides signals 38, 40 corresponding to a rising edge or increase in the FSK frequency and to a falling edge or decrease in the FSK frequency, respectively. The rising and falling edge signals 38, 40 are applied to a PLL 42 which synchronises itself with these edge signals and produces a recovered clock signal 44, substantially midway between detected the rising and falling edges.

A weakness in this typical clock recovery circuit 32 is that due to a group delay of the FSK frequencies in the transmitter 16 of the primary station 10 and/or in the presence of co-channel signals, there is a relative shifting between the rising and falling edges and the edges of a frictive signal in which all symbols are of equal length, which edges will hereinafter be referred to as "reference points(s)". In the secondary station, the edges in the demodulated NRZ data 30 do not occur at predetermined reference points but in regions either side of the reference points. The effect of this relative shifting is to cause the PLL 42 to advance or retard for each symbol change to align it with the predetermined reference point and this results in an increase of the PLL jitter and loss of sensitivity.

The vector diagram shown in Figure 3 shows the rising edges (advance) 46, the falling edges (retard) 47, the reference point 48 and the symbol clock 50 spaced 180 degrees apart from the reference point 48.

Figure 4A illustrates the original, uncorrupted NRZ data with each pulse having a nominal symbol period T seconds. Figure 4B illustrates the effect of group delay on the symbols such that the positive pulses are shorter by $\delta$ seconds than the period T, where $\delta$ is the time difference between the received symbol period and the ideal period T, whilst the negative pulses are longer by $\delta$ seconds than the period T. Nevertheless the rising and falling edges 46, 47 (or falling and rising edges) of the respective pulses are symmetrically disposed relative to the ideal period indicated by the reference points 48 and a time period of $\delta/2$ exists between the edge of the ideal period and the adjacent rising or falling edge. In accordance with the present invention the recovered clock can be generated from knowing at least the occurrence of the rising and falling

edges.

Referring to Figure 5, data 30 from the demodulator (not shown) is applied to an edge detector 36 which produces rising edge signals 38 and falling edge signals 40 which are applied to a first part 52 of a PLL 42 in which the value of δ is determined. The value is determined in an adaptive way by measuring the time between the rising and falling edges or vice versa. A proper integration constant enables variations of δ due to noise to be limited whilst at the same time permitting δ to be determined quickly enough not to miss data during synchronisation. In an embodiment of the present invention the edge detector 36 comprises a state machine which filters any noise close to the edges and calculates the midpoints between the edges.

A second part 54 of the PLL 42 receives not only the data edges 38, 40 but also δ and on the basis of δ, the part 54 calculates a reference position for the rising edges and another reference position for the falling edges. As a result of calculating these reference positions, the PLL 42 will not advance or retard for each symbol change because the active rising and falling edges are close to the respective calculated reference positions.

Figure 6 illustrates a vector diagram of a substantially jitter free PLL. The rising reference points (+δ/2) 56 and the falling reference points (-δ/2) 58 are disposed in the right hand half of the diagram and the recovered clock 50 is disposed in the left hand half of the diagram, symmetrically of the reference points 56, 58.

Having regard to Figure 5, the PLL 42 will advance only when an edge occurs after its reference position and will retard when an edge occurs before its reference position.

The circuit arrangement shown in Figure 5 enables jitter due to different symbol length to be greatly reduced without decreasing the bandwidth of the PLL. The lock time can be maintained fast not to miss synchronisation. Finally the requirement on the PLL reference oscillator is not stringent allowing the usage of cheaper crystals having a less stringent specification.

The embodiment of the invention illustrated in Figure 7 comprises an edge detector 36 which detects edges in the NRZ signal. The edge detector 36

generates a signal indicating a falling edge on an output 38 and a signal indicating a rising edge on an output 40. The outputs 38 and 40 are respectively connected to phase locked loops 60, 62. The phased locked loops 60, 62 are advanced respectively to align with the rising edge indication on the output 38 and with the falling edge indication on the output 40. The phases 64, 66 of the rising edge PLL 60 and the falling edge PLL 62, respectively, are fed into a stage 68 which calculates the mean phase of the PLLs and indicates a recovered clock when the mean of the phases is 180 degrees out of phase with respect to the reference points.

In operation when the rising edges lead the falling edges, the phases of the PLLs 60 and 62 will respectively have an offset of $\delta/2$ and - $\delta/2$ with respect to the reference points, as shown in Figure 8. Conversely, when the falling edges lead the rising edges, the phases of the PLLs 60, 62 will respectively have an offset of $\delta/2$ and $-\delta/2$ with respect to the reference points. By determining the mean of these two phases in the stage 68, the centre of the symbol will be accurately indicated with no error on an output 50.

The point at which the minimum circular mean of the phases 64 and 66 is 180 degrees out of phase with respect to the reference points can be calculated in a straight forward manner. Referring to Figure 9, the vectors 46 and 47 illustrate the phase values 64 and 66. If both PLLs 60 and 62 are configured such that 180 degrees indicates the point at which respective edges occur, and angles are expressed in the range (-180 degrees to 180 degrees), the recovered clock 50 should be indicated when the mean of phases is 0 degrees, i.e. when the output of PLL 60 equals minus the output of PLL 62 and both counters are in the range (-90 degrees to 90 degrees).

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the design, manufacture and use of receivers and component parts thereof and which may be used instead of or in addition to features already described herein.

Industrial Applicability

In any application, such as telecommunications, in which it is required to derive a clock signal from a data signal to be demodulated and detected.

CLAIMS

1. A receiver comprising receiving means for receiving a data signal and providing a base band output, demodulating means coupled to an output of the receiving means for providing a data output, and symbol recovery means coupled to an output of the demodulating means for recovering symbols represented by the data output, characterised in that the symbol recovery means comprises means for determining the occurrence of rising and falling edges in the data output, means for determining the differences between the occurrence of the rising and falling edges and means for utilising the differences for determining a clock reference position.

2. A receiver as claimed in claim 1, characterised in that said determining means comprises means for determining a time difference between rising and falling edges in the data output and their nominal reference points for producing a time difference signal, and in that phase locked loop means is provided having input means for the rising and falling edges and the time difference signal and means for calculating respective reference positions for the rising and falling edges.

3. A receiver as claimed in claim 2, characterised in that the time difference determining means is adapted to filter-out noise edges close to the rising and falling edges.

4. A receiver as claimed in claim 2 or 3, characterised in that the phase locked loop means has means for calculating a clock reference intermediate the respective reference positions for the rising and falling edges.

5. A receiver as claimed in claim 1, characterised in that respective rising and falling edge phase locked loop means are provided for determining the occurrence of a respective rising and falling edge positions, and in that means are provided for determining a clock reference position from a minimum

circular mean of the phases in the phase locked loop means.

6. A clock recovery circuit comprising means for determining the occurrence of rising and falling edges in a data signal, means for determining the differences between the occurrence of the rising and falling edges and means for utilising the differences for determining a clock reference position.

7. A circuit as claimed in claim 6, characterised in that said determining means comprises means for determining a time difference between rising and falling edges in the data signal and their nominal reference points for producing a time difference signal, and in that phase locked loop means is provided having input means for the rising and falling edges and the time difference signal and means for calculating respective reference positions for the rising and falling edges.

8. A circuit as claimed in claim 6, characterised in that respective rising and falling edge phase locked loop means are provided for determining the occurrence of a respective rising and falling edge positions, and in that means are provided for determining a clock reference position from a minimum circular mean of the phases in the phase locked loop means.

9. A method of recovering symbols in a data signal, comprising determining the occurrence of rising and falling edges in the data signal, determining the differences between the occurrence of the rising and falling edges, and utilising the differences for determining a clock reference position.

10. A method as claimed in claim 9, characterised in that phase locked loop means are used for determining a time difference between rising and falling edges in the data output and their nominal reference points for producing a time difference signal, and for calculating respective reference positions for the rising and falling edges from the time difference and the rising and falling edges.

11. A method as claimed in claim 9, characterised in that the occurrence of a respective rising and falling edge positions is determined by respective phase locked loop means, and in that a clock reference position is determined from a minimum circular mean of the phases in the phase locked loop means.

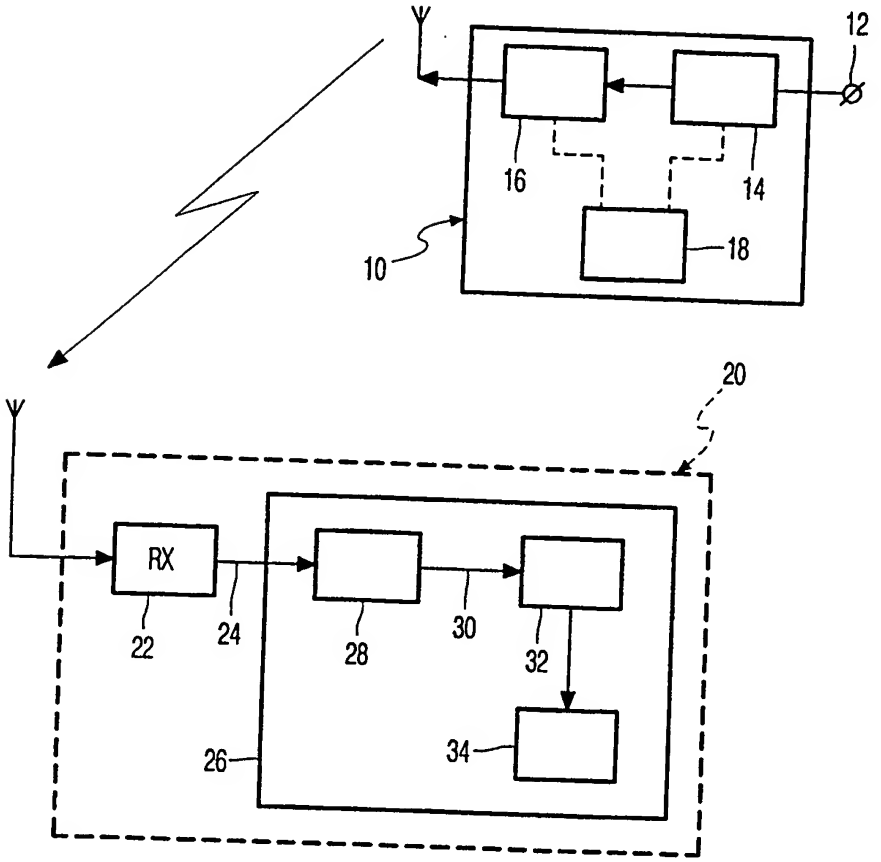


FIG. 1

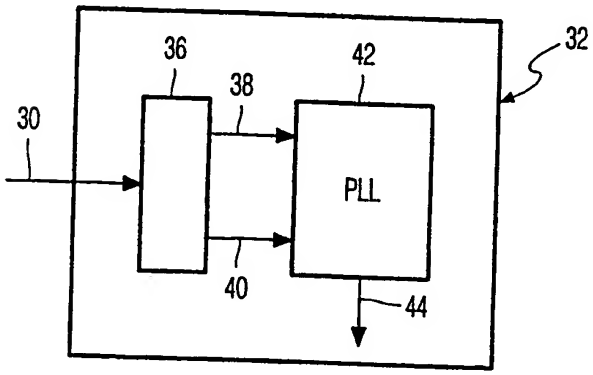


FIG. 2

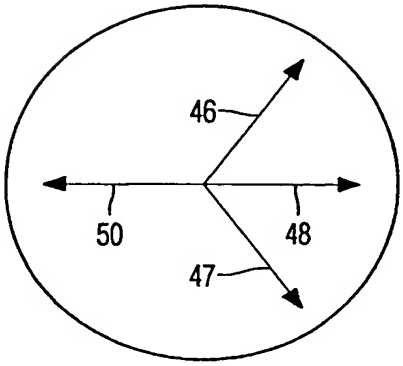


FIG. 3

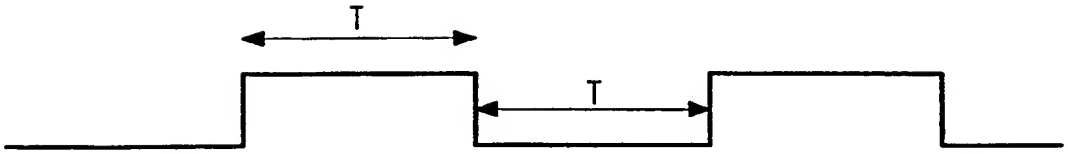


FIG. 4A

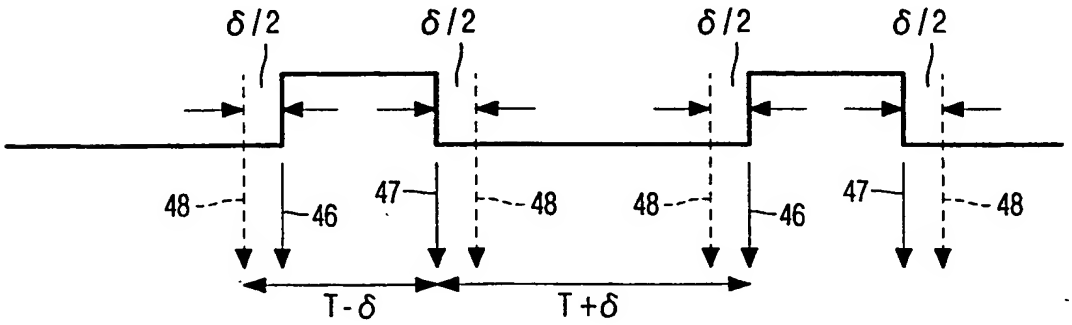


FIG. 4B

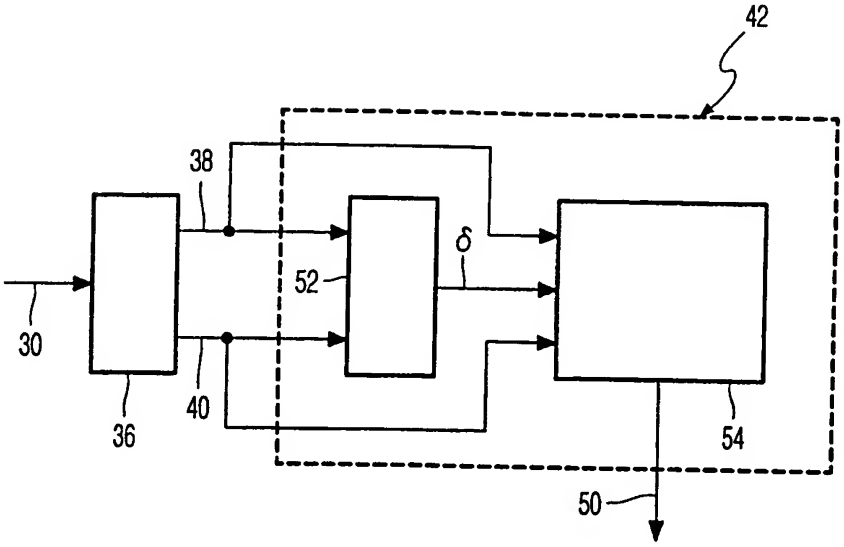


FIG. 5

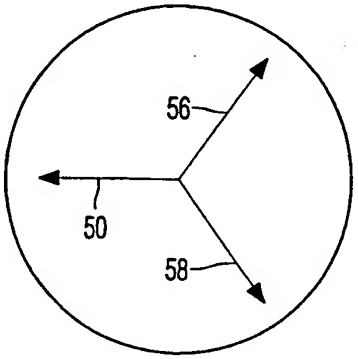


FIG. 6

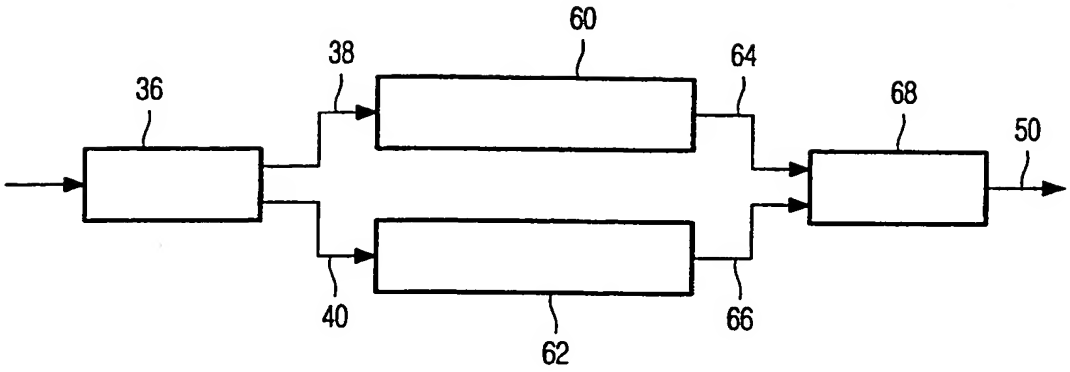


FIG. 7

FIG. 8

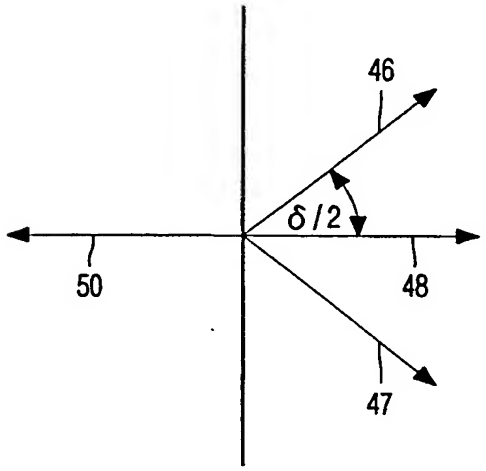


FIG. 9

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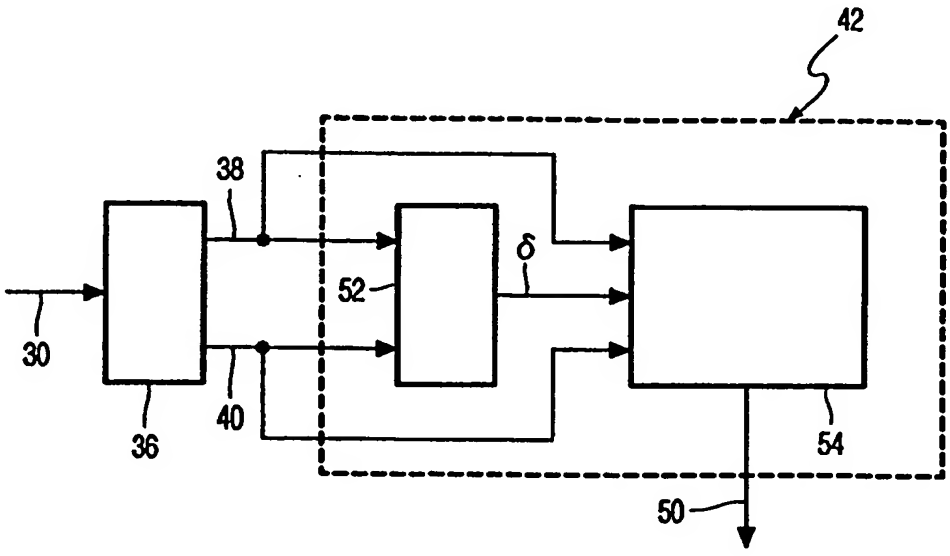


(57) Abstract

A data receiver comprises receiving means for receiving a data signal and providing a base band output, demodulating means coupled to an output of the receiving means for providing a data output, and symbol recovery means (36, 42) coupled to an output of the demodulating means for recovering symbols represented by the data output. The symbol recovery means comprises means (52) for determining a time difference between rising and falling edges in the data output and their nominal reference points and means (54) for determining respective clock reference points for the rising and falling edges from the time difference between the rising and falling edges.

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# INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 99/00264

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H04L 7/00
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPODOC, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| Y | US 5502711 A (ALAN R. CLARK ET AL), 26 March 1996 (26.03.96), column 7, line 29 - line 43; column 7, line 58 - column 8, line 29; column 8, line 48 - line 65, figures 3,4, claims 1-5, column 10, line 7 - line 18 | 1-11 |
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| Y | WO 9217967 A1 (MOTOROLA, INC.), 15 October 1992 (15.10.92), figure 3, claims 1,3-5,8,15 | 1-11 |
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| A | EP 0242576 B1 (INTERNATIONAL BUSINESS MACHINES CORPORATION), 27 Sept 1995 (27.09.95), claims 1-4, 6-7 | 1-11 |
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[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 13 October 1999 | 15-10-1999 |
| Name and mailing address of the ISA/<br>Swedish Patent Office<br>Box 5055, S-102 42 STOCKHOLM<br>Facsimile No. +46 8 666 02 86 | Authorized officer<br>Rickard Elg/cs<br>Telephone No. +46 8 782 25 00 |

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 99/00264

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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| A | US 4734900 A (NEIL R. DAVIE), 29 March 1988 (29.03.88), claims 1,4,6<br><br>--<br>-------- | 1-11 |

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Information on patent family members

28/09/99

International application No.
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